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## A robust platform cooled by superconducting electronic refrigerators

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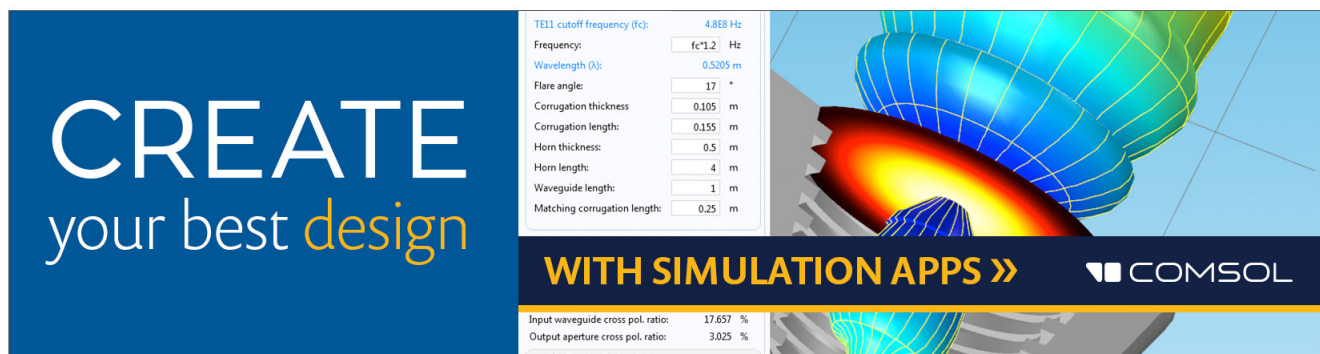
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Horn thickness:	0.5 m
Horn length:	4 m
Waveguide length:	1 m
Matching corrugation length:	0.25 m

Input waveguide cross pol. ratio: 17.657 %  
Output aperture cross pol. ratio: 3.025 %  
☒ Target criterion: passed

# A robust platform cooled by superconducting electronic refrigerators

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A biased tunnel junction between a superconductor and a normal metal can cool the latter electrode. Based on a recently developed cooler with high power and superior performance, we have integrated it with a dielectric silicon nitride membrane, and cooled phonons from 305 mK down to 200 mK. Without perforation and covered under a thin alumina layer, the membrane is rigorously transformed into a cooling platform that is robust and versatile for multiple practical purposes. We discussed our results and possibilities to further improve the device. © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4905440>]

Refrigeration below 1 K belongs traditionally to the domain of macroscopic machines, such as adiabatic demagnetization or <sup>3</sup>He-<sup>4</sup>He dilution cryostats. Although being reliable and universal, these systems are often bulky and complicated to operate. Alternatively, one can employ the cooling effect in a Normal Metal–Insulator–Superconductor (NIS) junction when such a contact is biased near the superconducting gap.<sup>1–8</sup> Powered by NIS coolers, a non-conducting platform can cool a transition edge sensor down to its working temperature<sup>9,10</sup> or it can ultimately replace a dilution unit.<sup>11</sup> This approach offers a simple, light weight solution to cool mesoscopic devices such as qubits,<sup>12</sup> nanomechanical resonators,<sup>13</sup> electron pumps,<sup>14</sup> or low temperature detectors,<sup>15</sup> especially those for spaceborne applications.<sup>16</sup>

There are many challenges that hinder an uncompromised demonstration of such a device. First, the Superconductor–Insulator–Normal metal–Insulator–Superconductor (SINIS) cooler under-performs its theoretical prediction, mainly due to the excessive number of injected quasiparticles in the superconducting lead.<sup>9–11,17</sup> On the other hand, those devices that would perform well, lack a practical power to handle external loads.<sup>4,7,18</sup> Second, when the device dimensions become comparable to the phonon wavelength, a few  $\mu\text{m}$  at low temperatures, size effects modify thermal transport properties,<sup>19</sup> especially at the boundary of materials.<sup>20</sup> It becomes increasingly difficult to precisely engineer the thermal transport, especially in the sub kelvin temperature regime. As a result, one often forces to suppress the thermal conductivity between the cold platform and its environment as effectively as possible. The platform of choice is an amorphous silicon nitride (SiN) membrane, where three dimensional phonons do not exist.<sup>21,22</sup> This two dimensional structure is then typically perforated so that the center part is suspended only by thin legs.<sup>9,21,23</sup> It results in a fragile structure and further manipulation is next to impossible, although there are outstanding exceptions.<sup>11</sup>

Recently, we have developed a SINIS electron cooler with a well thermalized superconductor using photolithography and wet etching.<sup>24,25</sup> This device has enough power to handle an external load, yet it performs outstandingly over a wide range of temperature.<sup>26</sup> In this paper, we demonstrate

an integration of these coolers on a SiN membrane. The platform reaches 200 mK from cryostat temperature of 305 mK without perforation of the membrane. With 1 nW cooling power at 300 mK, one pair of junctions is capable of cooling the membrane. We arrange three other auxiliary coolers that power other coldfingers arranged in an “onion” like configuration to shunt part of the heat from the external bath.

Following the technique in Refs. 24 and 25, the fabrication starts by depositing a multilayer on a low stress SiN membrane of size  $1\text{ mm} \times 1\text{ mm} \times 100\text{ nm}$ .<sup>27</sup> Respectively, 200 nm of AlMn, 200 nm of Al, and 60 nm of Cu are sputtered *in situ* with oxidations in between. The AlMn layer, which is normal,<sup>25</sup> is oxidized in a mixture of Ar:O<sub>2</sub> of ratio 10:1 at  $2 \times 10^{-2}$  mbar pressure for 2 min, and the Al layer in pure O<sub>2</sub> at 7 mbar for 5 min. Two photolithography steps<sup>24</sup> with wet etching of Cu and Al then follow to define the four coolers, which are aligned to corners of the membrane. The size of a NIS junction is  $200 \times 4\text{ }\mu\text{m}^2$  and a cooler has 1 nW cooling power at 300 mK. The normal island of the SINIS has a pair of smaller NIS junctions to probe its temperature, see lower left side of Fig. 1(a).

Next, four coldfingers are patterned using electron beam lithography, and 60 nm of Cu is deposited with a lift-off resist scheme. These coldfingers connect the cold normal metal to the center of the membrane. They are designed so that there is one main coldfinger, one middle coldfinger, and two outer coldfingers (see Fig. 3 for different designs). The whole device is then covered by 25 nm of AlO<sub>x</sub> using atomic layer deposition (ALD) with H<sub>2</sub>O and Al(CH<sub>3</sub>)<sub>3</sub> as precursors at pressure 5 mbar and temperature 100 °C. This passive layer isolates the cooler electrically from any structure patterned above it. Besides electron thermometers attached to the cooler itself, SINIS thermometers are placed at various places using electron beam lithography and two angle evaporation. These thermometers are isolated through the alumina layer and read local phonon temperatures. Note that this production step is totally independent from the cooler fabrication and employs state of the art electron beam lithography. Consequently, fabrication of other devices is feasible following this recipe. As we need a normal metal for our SINIS thermometer, the angle of copper deposition is large (50°) so

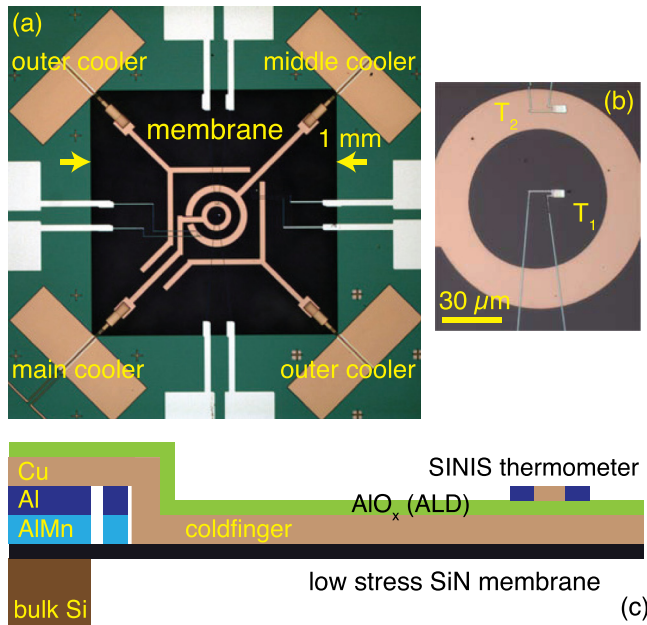


FIG. 1. (a) Layout of the cooling platform equipped with four SINIS coolers at corners of the low stress SiN membrane. One NIS junction has an overlap area of  $200 \times 4 \mu\text{m}^2$ , and the membrane size is  $1 \times 1 \text{ mm}^2$ . The coldfingers are arranged in such a way that the main coldfinger is surrounded by three others to shunt the leak from the bulk. (b) Zoom of the middle part in (a) that shows a SINIS thermometer at the center of the membrane and another one on top of the coldfinger. (c) Cross-sectional diagram of the device. The cooler with an AlMn quasiparticle drain and a suspended Cu layer is connected to the Cu-only coldfinger that extends to the center of the SiN membrane. The whole device is covered under a thin alumina AIO<sub>x</sub> layer. A small SINIS thermometer probes the phonon temperature at the center of the membrane.

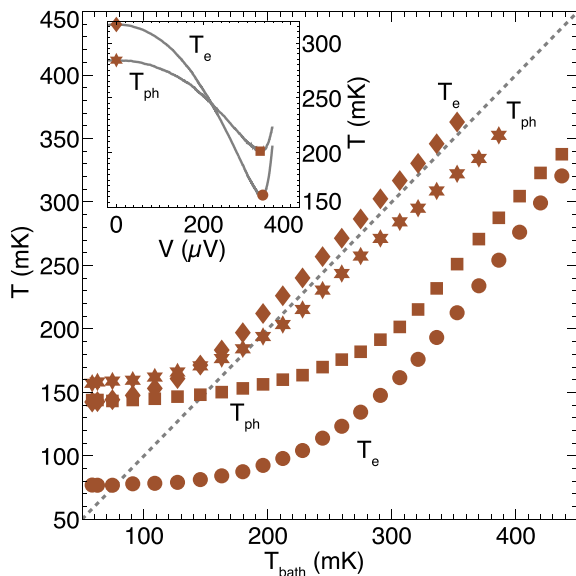


FIG. 2. Temperatures at different parts of the device as a function of bath temperature when all outer coolers are biased optimally. Diamonds show the temperature of the main cooler at zero bias, which is also the bulk phonon temperature on the chip. Stars show the phonon temperature at the center of the membrane when the main cooler is at zero bias. Squares represent the main result of this work, the lowest phonon temperature on the membrane, and circles are the lowest electron temperature of the main cooler. The dashed line yields  $T = T_{\text{bath}}$ . The inset shows data at 305 mK bath temperature as a function of bias on the main cooler when other coolers are optimally biased.

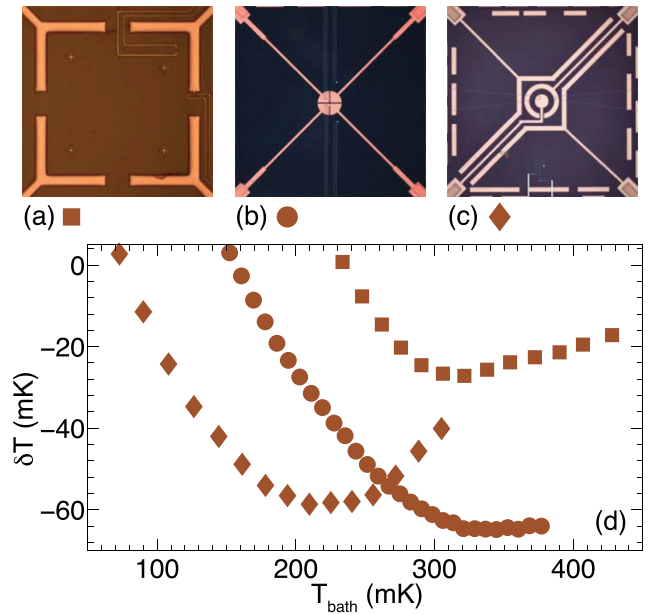


FIG. 3. (a)–(c) Different layouts of the coldfinger. The membrane appears as dark color, and the Cu coldfinger as bright color. Each image covers an area of  $850 \times 850 \mu\text{m}^2$ . (d) Phonon temperature at the center of the membrane corresponding to samples (a)–(c). Note that (c) is similar to that in Fig. 2 but with an inferior performance.

that Cu along the connecting lines falls on the wall of the resist and is removed during lift off. The resulting superconducting Al-only wires on the membrane ensure low thermal contact to the outside. During the whole fabrication, temperature is limited to  $130^\circ\text{C}$  to protect the top Cu layer from oxidation as well as to warrant the quality of the tunnel barrier.

The sample is then glued to the stage at the mixing chamber of a dilution cryostat. About 30 gold wires of diameter  $25 \mu\text{m}$  are bonded around the device from the chip to the sample stage to enhance thermalization of the coolers. Due to the limited number of wires in the cryostat, only the main cooler, which is connected to the centermost coldfinger, is bonded with four wires. The other three coolers are bonded in series and are run independently of the main one. This way, the optimum bias of the whole device is determined by iteratively searching for the optimum of each cooler based on the performance at the center of the membrane of the whole device. This is done automatically using a Matlab script. In other experiments that are not reported here, bonding four coolers either in series or in parallel gave, as expected, similar cooling performance at the center of the membrane. The SINIS thermometers are calibrated to the cryostat temperature when all coolers are unbiased. Throughout this work, bath temperatures of the cryostat are read with a ruthenium oxide resistor calibrated against a Coulomb blockade thermometer.<sup>28</sup> The bath temperature is not necessarily equal to the chip temperature (see Fig. 2, diamond symbols), as the latter can be significantly elevated due to the high input power of the cooler of about 100 nW.

Performance of the device at bath temperature 305 mK is shown in the inset of Fig. 2 when three outer coolers are set to their optimum bias points.  $T_e$  shows the electron temperature of the cooler on bulk, and  $T_{\text{ph}}$  the phonon temperature at the center of the membrane. At zero bias on the main



cooler,  $T_e$  reads temperature of the bulk, which is overheated to 317 mK, diamond symbol, due to the high input current  $\sim 90 \mu\text{A}$  on three other coolers. However, the center of the membrane is cooled to 285 mK, star symbol, due to the three cooled coldfingers, even when the main coldfinger is thermalized to the bath temperature on bulk. At the optimum bias on the main cooler, the center of the membrane is cooled to 200 mK, square symbol. The main figure presents the same data at the optimum working bias versus bath temperature. In general, the chip is always overheated, and the membrane is effectively cooled with extra help from the auxiliary coolers. At optimum cooling, phonon temperature on the membrane reaches 150 mK from 250 mK, which is an achievable base temperature of a  $^3\text{He}$  cryostat. This temperature is quite uniform in this area as the thermometer at the center and the one on top of the coldfinger ( $T_1$  and  $T_2$  in Fig. 1(b)) show almost the same value (data not shown). Although electrons on the main cooler reach 60 mK similar to the case on bulk,<sup>26</sup> phonons on the membrane saturate at about 150 mK mainly due to the residual heat leak on it and weak electron-phonon interactions in the coldfinger at low temperature ( $\dot{Q}_{e-ph} \propto T_{ph}^5$ ).

We have investigated different layouts of the coldfinger. In all these tests, the membranes are unperforated. A similar design to the device reported in Ref. 9 with a Y shaped coldfinger in Fig. 3(a): phonons on the membrane reach 270 mK from 300 mK bath temperature, see square symbols in Fig. 3(d). Note that this sample was not covered with  $\text{AlO}_x$  by ALD, and there is a gap between coldfingers for wiring of the thermometers. Apparently, heat leak to the membrane is large. Figure 3(b) presents another approach, where four coolers play an equal role, and all are connected to a “cold disc” at the center of the membrane. The cold disc should cool the sample on top more efficiently as compared to a piece of membrane that is surrounded by the coldfinger, like the one in Fig. 1(a). Separated through the thin alumina layer, the thermometer on top of this cold disc reaches only 240 mK from the bath temperature of 300 mK (circle symbols), even though the coolers perform similarly to the one presented in Fig. 2. Figure 3(c) presents a similar design as the sample of Fig. 1(a) except that the center part is a cold disc and one cooling junction has an area of  $70 \times 4 \mu\text{m}^2$ . The smaller junction generates less heat on the chip, but provides less cooling power as well. As a result, this particular device works well at low temperatures, but loses its power near 300 mK.

Heuristically, the onion-like coldfinger should work better than the regular design, e.g., the Y-shape used in Ref. 9. Here, the outer coldfinger precools the inside area and at the same time prevents the external heat load. The inner coldfinger, now precooled to a temperature lower than the bath, can focus on cooling just a small part of the membrane. This is possible because each cooler has 1 nW power at 300 mK, enough to cool the whole membrane. Of course, it is more desirable to cool the whole inner cooler directly with the outer cooler, similar to a cascade cooler.<sup>29</sup> Such a setup requires the superconducting electrodes to be on the membrane, which generates a lot of heat and poses even more challenges.

We have focused on a practical platform that is suitable for a wide range of applications. To start with, it is not perforated. A robust SiN membrane with excellent mechanical properties would survive further integration with other devices. For example, fabrication of a kinetic inductance device or a qubit on it would be quite straightforward following the demonstrated fabrication scheme. Second, the whole platform is passivated with alumina, isolating the foreseen cooled device on top. The passivated alumina layer also allows a free design of the coldfinger layout as required by different applications. These two advances transform the SiN membrane into a robust and versatile platform. Last but not least, the cooler has a high power and can thus accommodate for dissipative devices on top. This platform would provide a phonon bath of 150 mK when attached to a  $^3\text{He}$  adsorption cryostat.

The presented cooler dissipates a large amount of heat in the surroundings of the membrane, up to  $1 \mu\text{W}$ . Although bonding extra gold wires improves thermalization, as reflected on the improved phonon temperature of the membrane (data not shown), this is kind of a hasty solution to the on-chip overheating issue. A more systematic approach of the whole set up is desired, such as using gold ribbon, and clamping the device to the sample stage. Moreover, each cooler should focus on its own task. The outer cooler should aim at high power to shunt the heat leak, and the inner cooler should seek for high performance, either by reducing the size of the cooling junction or by increasing the tunnel barrier thickness for a weaker overheating of the superconducting electrode.<sup>26</sup> Additionally, other material choices, such as nano-perforated,<sup>30,31</sup> nano-laminated,<sup>32,33</sup> or corrugated membranes,<sup>34,35</sup> might also enhance thermal isolation between the cold and the hot regions. Finally, the cryostat used for the present measurement had a small power that was barely enough to support the high input current of the device (200  $\mu\text{A}$ ).

In conclusion, we have transformed a standard commercial SiN membrane into a cooling platform by integrating it with powerful SINIS refrigerators. Phonons at the center of the membrane reach 150 mK from 250 mK starting temperature, the base temperature of a  $^3\text{He}$  cryostat. This passivated, unperforated platform is compatible with a wide range of requirements set by practical implementations.

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